IBM
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March 11, 2010

Mr. Roger Bowler
President
TurboHercules SAS
Tour Arane, 33eme etage
5, Place de la Pyramide
La Defense 9
92088 PARIS LA DEFENSE
FRANCE

Re: TurboHercules

Dear Mr. Bowler:

We have received and considered your letter of November 18, 2009. The comments you provide do not lead IBM to reconsider IBM's position as set out in my letter of November 4, 2009. Your suggestion that TurboHercules was unaware that IBM has intellectual property rights in this area is surprising. IBM has spent many years and many billions of dollars developing its z-architecture and technology, and is widely known to have many intellectual property rights in this area. IBM's litigation against PSI for, among other things, patent infringement and trade secret misappropriation is a matter of public record, and well known in the industry. According to your own statements, your product emulates significant portions of IBM's proprietary instruction set architecture and IBM has many patents that would, therefore, be infringed. For illustration, I enclose with this letter a non-exhaustive list of IBM U.S. patents that protect innovative elements of IBM's mainframe architecture and that IBM believes will be infringed by an emulator covering those elements. For your information, the enclosed list also includes a non-exhaustive list of relevant IBM U.S. published patent applications. Apart from concerns about unauthorized use of proprietary IBM information by one or more TurboHercules contributors, IBM therefore has substantial concerns about infringement of patented IBM technology. In these circumstances, I trust you will understand that IBM cannot agree to your request to reconsider its position.

Sincerely,

Mark S. Anzani

Mark S. Anzani
VP and Chief Technology Officer, IBM System z

Non-Exhaustive List of IBM U.S. Patents and IBM U.S. Published Patent Applications

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
1.	7,624,237	INSTRUCTION SET ARCHITECTURE	COMPARE, SWAP AND STORE FACILITY WITH NO EXTERNAL SERIALIZATION
2.	7,617,410	PARALLEL SYSPLEX ARCHITECTURE	SIMULTANEOUSLY UPDATING LOGICAL TIME OF DAY (TOD) CLOCKS FOR MULTIPLE CPUS IN RESPONSE TO DETECTING A CARRY AT A PRE-DETERMINED BIT POSITION OF A PHYSICAL CLOCK
3.	7,600,053	CHANNEL SUBSYSTEM ARCHITECTURE	EMULATION OF EXTENDED INPUT/OUTPUT MEASUREMENT BLOCK FACILITIES
4.	7,594,094	INSTRUCTION SET ARCHITECTURE	MOVE DATA FACILITY WITH OPTIONAL SPECIFICATIONS
5.	7,587,531	CHANNEL SUBSYSTEM ARCHITECTURE	MULTIPLE LOGICAL INPUT/OUTPUT SUBSYSTEM FACILITY
6.	7,581,074	MEMORY ARCHITECTURE	FACILITATING USE OF STORAGE ACCESS KEYS TO ACCESS STORAGE
7.	7,543,095	VIRTUALIZATION ARCHITECTURE	MANAGING INPUT/OUTPUT INTERRUPTIONS IN NON-DEDICATED INTERRUPTION HARDWARE ENVIRONMENTS
8.	7,516,304	INSTRUCTION SET ARCHITECTURE	PARSING-ENHANCEMENT FACILITY
9.	7,500,084	INSTRUCTION SET ARCHITECTURE	MULTIFUNCTION HEXADECIMAL INSTRUCTION FORM
10.	7,454,548	VIRTUALIZATION ARCHITECTURE	MANAGING INPUT/OUTPUT INTERRUPTIONS IN NON-DEDICATED INTERRUPTION HARDWARE ENVIRONMENTS, AND METHODS THEREFOR
11.	7,395,448	PARALLEL SYSPLEX ARCHITECTURE	DIRECTLY OBTAINING BY APPLICATION PROGRAMS INFORMATION USABLE IN DETERMINING CLOCK ACCURACY
12.	7,380,041	VIRTUALIZATION ARCHITECTURE	MANAGING INPUT/OUTPUT INTERRUPTIONS IN NON-DEDICATED INTERRUPTION HARDWARE ENVIRONMENTS
13.	7,373,435	CHANNEL SUBSYSTEM ARCHITECTURE	EXTENDED INPUT/OUTPUT MEASUREMENT BLOCK
14.	7,356,725	INSTRUCTION SET ARCHITECTURE	METHOD AND APPARATUS FOR ADJUSTING A TIME OF DAY CLOCK WITHOUT ADJUSTING THE STEPPING RATE OF AN OSCILLATOR
15.	7,356,710	INSTRUCTION SET ARCHITECTURE	SECURITY MESSAGE AUTHENTICATION CONTROL INSTRUCTION
16.	7,290,070	CHANNEL SUBSYSTEM ARCHITECTURE	MULTIPLE LOGICAL INPUT/OUTPUT SUBSYSTEM FACILITY
17.	7,284,100	INSTRUCTION SET ARCHITECTURE	INVALIDATING STORAGE, CLEARING BUFFER ENTRIES, AND AN INSTRUCTION THEREFOR
18.	7,281,115	MEMORY ARCHITECTURE	METHOD, SYSTEM AND PROGRAM PRODUCT FOR CLEARING SELECTED STORAGE TRANSLATION BUFFER ENTRIES
19.	7,257,718	INSTRUCTION SET ARCHITECTURE	CIPHER MESSAGE ASSIST INSTRUCTIONS
20.	7,254,698	INSTRUCTION SET ARCHITECTURE	MULTIFUNCTION HEXADECIMAL INSTRUCTIONS
21.	7,197,601	MEMORY ARCHITECTURE	METHOD, SYSTEM AND PROGRAM PRODUCT FOR INVALIDATING A RANGE OF SELECTED STORAGE TRANSLATION TABLE ENTRIES
22.	7,197,585	VIRTUALIZATION	METHOD AND APPARATUS FOR MANAGING THE

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
		ARCHITECTURE	EXECUTION OF A BROADCAST INSTRUCTION ON A GUEST PROCESSOR
23.	7,174,550	CHANNEL SUBSYSTEM ARCHITECTURE	SHARING COMMUNICATIONS ADAPTERS ACROSS A PLURALITY OF INPUT/OUTPUT SUBSYSTEM IMAGES
24.	7,174,274	CHANNEL SUBSYSTEM ARCHITECTURE	GATHERING I/O MEASUREMENT DATA DURING AN I/O OPERATION PROCESS
25.	7,159,122	INSTRUCTION SET ARCHITECTURE	MESSAGE DIGEST INSTRUCTIONS
26.	7,146,523	PARALLEL SYSPLEX ARCHITECTURE	MONITORING PROCESSING MODES OF COUPLING FACILITY STRUCTURES
27.	7,130,949	VIRTUALIZATION ARCHITECTURE	MANAGING INPUT/OUTPUT INTERRUPTIONS IN NON-DEDICATED INTERRUPTION HARDWARE ENVIRONMENTS
28.	7,127,599	CHANNEL SUBSYSTEM ARCHITECTURE	MANAGING CONFIGURATIONS OF INPUT/OUTPUT SYSTEM IMAGES OF AN INPUT/OUTPUT SUBSYSTEM, WHEREIN A CONFIGURATION IS MODIFIED WITHOUT RESTARTING THE INPUT/OUTPUT SUBSYSTEM TO EFFECT A MODIFICATION
29.	7,058,837	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND SYSTEM FOR PROVIDING A MESSAGE-TIME-ORDERING FACILITY
30.	7,013,305	PARALLEL SYSPLEX ARCHITECTURE	MANAGING THE STATE OF COUPLING FACILITY STRUCTURES, DETECTING BY ONE OR MORE SYSTEMS COUPLED TO THE COUPLING FACILITY, THE SUSPENDED STATE OF THE DUPLEXED COMMAND, DETECTING BEING INDEPENDENT OF MESSAGE EXCHANGE
31.	7,003,700	PARALLEL SYSPLEX ARCHITECTURE	HALTING EXECUTION OF DUPLEXED COMMANDS
32.	7,000,036	CHANNEL SUBSYSTEM ARCHITECTURE	EXTENDED INPUT/OUTPUT MEASUREMENT FACILITIES
33.	6,996,638	CHANNEL SUBSYSTEM ARCHITECTURE	METHOD, SYSTEM AND PROGRAM PRODUCTS FOR ENHANCING INPUT/OUTPUT PROCESSING FOR OPERATING SYSTEM IMAGES OF A COMPUTING ENVIRONMENT
34.	6,971,002	PARTITIONING	METHOD, SYSTEM, AND PRODUCT FOR BOOTING A PARTITION USING ONE OF MULTIPLE, DIFFERENT FIRMWARE IMAGES WITHOUT REBOOTING OTHER PARTITIONS
35.	6,963,940	CHANNEL SUBSYSTEM ARCHITECTURE	MEASURING UTILIZATION OF INDIVIDUAL COMPONENTS OF CHANNELS
36.	6,963,882	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR PROCESSING A LIST STRUCTURE
37.	6,944,787	PARALLEL SYSPLEX ARCHITECTURE	SYSTEM-MANAGED DUPLEXING OF COUPLING FACILITY STRUCTURES
38.	6,862,595	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR IMPLEMENTING A SHARED MESSAGE QUEUE USING A LIST STRUCTURE
39.	6,859,866	PARALLEL SYSPLEX ARCHITECTURE	SYNCHRONIZING PROCESSING OF COMMANDS INVOKED AGAINST DUPLEXED COUPLING FACILITY STRUCTURES
40.	6,813,726	PARALLEL SYSPLEX ARCHITECTURE	RESTARTING A COUPLING FACILITY COMMAND USING A TOKEN FROM ANOTHER COUPLING FACILITY COMMAND
41.	6,775,789	INSTRUCTION SET	METHOD, SYSTEM AND PROGRAM PRODUCTS

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
		ARCHITECTURE	FOR GENERATING SEQUENCE VALUES THAT ARE UNIQUE ACROSS OPERATING SYSTEM IMAGES
42.	6,748,460	CHANNEL SUBSYSTEM ARCHITECTURE	INITIATIVE PASSING IN AN I/O OPERATION WITHOUT THE OVERHEAD OF AN INTERRUPT
43.	6,714,997	VIRTUALIZATION ARCHITECTURE	METHOD AND MEANS FOR ENHANCED INTERPRETIVE INSTRUCTION EXECUTION FOR A NEW INTEGRATED COMMUNICATIONS ADAPTER USING A QUEUED DIRECT INPUT-OUTPUT DEVICE
44.	6,687,853	CHANNEL SUBSYSTEM ARCHITECTURE	CHECKPOINTING FOR RECOVERY OF CHANNELS IN A DATA PROCESSING SYSTEM
45.	6,681,238	VIRTUALIZATION ARCHITECTURE	METHOD AND SYSTEM FOR PROVIDING A HARDWARE MACHINE FUNCTION IN A PROTECTED VIRTUAL MACHINE
46.	6,654,812	PARTITIONING	COMMUNICATION BETWEEN MULTIPLE PARTITIONS EMPLOYING HOST-NETWORK INTERFACE
47.	6,615,373	PARALLEL SYSPLEX ARCHITECTURE	METHOD, SYSTEM AND PROGRAM PRODUCTS FOR RESOLVING POTENTIAL DEADLOCKS
48.	6,609,214	PARALLEL SYSPLEX ARCHITECTURE	METHOD, SYSTEM AND PROGRAM PRODUCTS FOR COPYING COUPLING FACILITY STRUCTURES
49.	6,598,069	PARTITIONING	METHOD AND APPARATUS FOR ASSIGNING RESOURCES TO LOGICAL PARTITION CLUSTERS
50.	6,594,667	PARALLEL SYSPLEX ARCHITECTURE	METHOD, SYSTEM AND PROGRAM PRODUCTS FOR MODIFYING COUPLING FACILITY STRUCTURES
51.	6,584,554	PARALLEL SYSPLEX ARCHITECTURE	DIRECTED ALLOCATION OF COUPLING FACILITY STRUCTURES
52.	6,567,841	PARTITIONING	METHOD AND APPARATUS FOR CREATING AND IDENTIFYING LOGICAL PARTITION CLUSTERS
53.	6,539,495	PARALLEL SYSPLEX ARCHITECTURE	METHOD, SYSTEM AND PROGRAM PRODUCTS FOR PROVIDING USER-MANAGED DUPLEXING OF COUPLING FACILITY CACHE STRUCTURES
54.	6,438,654	PARALLEL SYSPLEX ARCHITECTURE	CASTOUT PROCESSING FOR DUPLEXED CACHE STRUCTURES
55.	6,345,329	CHANNEL SUBSYSTEM ARCHITECTURE	METHOD AND APPARATUS FOR EXCHANGING DATA USING A QUEUED DIRECT INPUT-OUTPUT DEVICE
56.	6,339,802	CHANNEL SUBSYSTEM ARCHITECTURE	COMPUTER PROGRAM DEVICE AND AN APPARATUS FOR PROCESSING OF DATA REQUESTS USING A QUEUED DIRECT INPUT-OUTPUT DEVICE
57.	6,336,184	INSTRUCTION SET ARCHITECTURE	METHOD AND APPARATUS FOR PERFORMING A TRAP OPERATION IN AN INFORMATION HANDLING SYSTEM
58.	6,332,171	CHANNEL SUBSYSTEM ARCHITECTURE	SELF-CONTAINED QUEUES WITH ASSOCIATED CONTROL INFORMATION FOR RECEIPT AND TRANSFER OF INCOMING AND OUTGOING DATA USING A QUEUED DIRECT INPUT-OUTPUT DEVICE
59.	6,237,000	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR PREVIEWING THE RESULTS OF A DATA STRUCTURE ALLOCATION
60.	6,209,106	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR SYNCHRONIZING SELECTED LOGICAL PARTITIONS OF A PARTITIONED INFORMATION HANDLING SYSTEM TO AN EXTERNAL TIME REFERENCE

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
61.	6,189,007	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR CONDUCTING A HIGH PERFORMANCE LOCKING FACILITY IN A LOOSELY COUPLED ENVIRONMENT
62.	6,085,313	INSTRUCTION SET ARCHITECTURE	COMPUTER PROCESSOR SYSTEM FOR EXECUTING RXE FORMAT FLOATING POINT INSTRUCTIONS
63.	6,009,261	EMULATION	PREPROCESSING OF STORED TARGET ROUTINES FOR EMULATING INCOMPATIBLE INSTRUCTIONS ON A TARGET PROCESSOR
64.	5,987,495	INSTRUCTION SET ARCHITECTURE	METHOD AND APPARATUS FOR FULLY RESTORING A PROGRAM CONTEXT FOLLOWING AN INTERRUPT
65.	5,953,520	EMULATION	ADDRESS TRANSLATION BUFFER FOR DATA PROCESSING SYSTEM EMULATION MODE
66.	5,923,890	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR OPTIMIZING THE HANDLING OF SYNCHRONOUS REQUESTS TO A COUPLING FACILITY IN A SYSPLEX CONFIGURATION
67.	5,893,157	INSTRUCTION SET ARCHITECTURE	BLOCKING SYMBOL CONTROL IN A COMPUTER SYSTEM TO SERIALIZE ACCESSING A DATA RESOURCE BY SIMULTANEOUS PROCESSOR REQUESTS
68.	5,887,135	PARALLEL SYSPLEX ARCHITECTURE	SYSTEM AND METHOD FOR MANAGEMENT OF OBJECT TRANSITIONS IN AN EXTERNAL STORAGE FACILITY ACCESSED BY ONE OR MORE PROCESSORS
69.	5,875,484	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND SYSTEM FOR DETERMINING AND OVERRIDING INFORMATION UNAVAILABILITY TIME AT A COUPLING FACILITY
70.	5,875,336	EMULATION	METHOD AND SYSTEM FOR TRANSLATING A NON-NATIVE BYTECODE TO A SET OF CODES NATIVE TO A PROCESSOR WITHIN A COMPUTER SYSTEM
71.	5,860,115	PARALLEL SYSPLEX ARCHITECTURE	REQUESTING A DUMP OF INFORMATION STORED WITHIN A COUPLING FACILITY, IN WHICH THE DUMP INCLUDES SERVICEABILITY INFORMATION FROM AN OPERATING SYSTEM THAT LOST COMMUNICATION WITH THE COUPLING FACILITY
72.	5,825,678	INSTRUCTION SET ARCHITECTURE	METHOD AND APPARATUS FOR DETERMINING FLOATING POINT DATA CLASS
73.	5,822,562	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR EXPANSION, CONTRACTION, AND REAPPORTIONMENT OF STRUCTURED EXTERNAL STORAGE STRUCTURES
74.	5,761,739	PARALLEL SYSPLEX ARCHITECTURE	METHODS AND SYSTEMS FOR CREATING A STORAGE DUMP WITHIN A COUPLING FACILITY OF A MULTISYSTEM ENVIROMENT
75.	5,745,676	INSTRUCTION SET ARCHITECTURE	AUTHORITY REDUCTION AND RESTORATION METHOD PROVIDING SYSTEM INTEGRITY FOR SUBSPACE GROUPS AND SINGLE ADDRESS SPACES DURING PROGRAM LINKAGE
76.	5,742,830	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR PERFORMING CONDITIONAL OPERATIONS ON EXTERNALLY SHARED DATA
77.	5,706,432	PARALLEL SYSPLEX ARCHITECTURE	MECHANISM FOR RECEIVING MESSAGES AT A COUPLING FACILITY
78.	5,704,055	OTHER ARCHITECTURE	DYNAMIC RECONFIGURATION OF MAIN

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
			STORAGE AND EXPANDED STORAGE BY MEANS OF A SERVICE CALL LOGICAL PROCESSOR
79.	5,696,709	INSTRUCTION SET ARCHITECTURE	PROGRAM CONTROLLED ROUNDING MODES
80.	5,687,106	OTHER ARCHITECTURE	IMPLEMENTATION OF BINARY FLOATING POINT USING HEXADECIMAL FLOATING POINT UNIT
81.	5,636,373	PARALLEL SYSPLEX ARCHITECTURE	SYSTEM FOR SYNCHRONIZING LOGICAL CLOCK IN LOGICAL PARTITION OF HOST PROCESSOR WITH EXTERNAL TIME SOURCE BY COMBINING CLOCK ADJUSTMENT VALUE WITH SPECIFIC VALUE OF PARTITION
82.	5,630,050	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND SYSTEM FOR CAPTURING AND CONTROLLING ACCESS TO INFORMATION IN A COUPLING FACILITY
83.	5,613,086	INSTRUCTION SET ARCHITECTURE	METHOD AND SYSTEM FOR LOCKING A PAGE OF REAL STORAGE USING A VIRTUAL ADDRESS
84.	5,581,737	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR EXPANSION, CONTRACTION, AND REAPPORTIONMENT OF STRUCTURED EXTERNAL STORAGE STRUCTURES
85.	5,574,945	PARALLEL SYSPLEX ARCHITECTURE	MULTI CHANNEL INTER-PROCESSOR COUPLING FACILITY PROCESSING RECEIVED COMMANDS STORED IN MEMORY ABSENT STATUS ERROR OF CHANNELS
86.	5,574,938	PARALLEL SYSPLEX ARCHITECTURE	ALLOWED OPERATIONAL-LINK TRANSCEIVER TABLE VERIFIES THE OPERATIONAL STATUS OF TRANSCEIVERS IN A MULTIPLE CONDUCTOR DATA TRANSMISSION LINK
87.	5,561,809	PARALLEL SYSPLEX ARCHITECTURE	IN A MULTIPROCESSING SYSTEM HAVING A COUPLING FACILITY, COMMUNICATING MESSAGES BETWEEN THE PROCESSORS AND THE COUPLING FACILITY IN EITHER A SYNCHRONOUS OPERATION OR AN ASYNCHRONOUS OPERATION
88.	5,544,345	PARALLEL SYSPLEX ARCHITECTURE	COHERENCE CONTROLS FOR STORE-MULTIPLE SHARED DATA COORDINATED BY CACHE DIRECTORY ENTRIES IN A SHARED ELECTRONIC STORAGE
89.	5,493,668	PARALLEL SYSPLEX ARCHITECTURE	MULTIPLE PROCESSOR SYSTEM HAVING SOFTWARE FOR SELECTING SHARED CACHE ENTRIES OF AN ASSOCIATED CASTOUT CLASS FOR TRANSFER TO A DASD WITH ONE I/O OPERATION
90.	5,493,661	INSTRUCTION SET ARCHITECTURE	METHOD AND SYSTEM FOR PROVIDING A PROGRAM CALL TO A DISPATCHABLE UNIT'S BASE SPACE
91.	5,463,736	PARALLEL SYSPLEX ARCHITECTURE	COUPLING FACILITY FOR RECEIVING COMMANDS FROM PLURALITY OF HOSTS FOR ACTIVATING SELECTED CONNECTION PATHS TO I/O DEVICES AND MAINTAINING STATUS THEREOF
92.	5,452,455	CHANNEL SUBSYSTEM ARCHITECTURE	ASYNCHRONOUS COMMAND SUPPORT FOR SHARED CHANNELS FOR A COMPUTER COMPLEX HAVING MULTIPLE OPERATING SYSTEMS
93.	5,450,590	PARALLEL SYSPLEX ARCHITECTURE	AUTHORIZATION METHOD FOR CONDITIONAL COMMAND EXECUTION
94.	5,442,350	OTHER ARCHITECTURE	METHOD AND MEANS PROVIDING STATIC DICTIONARY STRUCTURES FOR COMPRESSING

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
			CHARACTER DATA AND EXPANDING COMPRESSED DATA
95.	5,416,921	PARALLEL SYSPLEX ARCHITECTURE	APPARATUS AND ACCOMPANYING METHOD FOR USE IN A SYSPLEX ENVIRONMENT FOR PERFORMING ESCALATED ISOLATION OF A SYSPLEX COMPONENT IN THE EVENT OF A FAILURE
96.	5,414,851	PARTITIONING	METHOD AND MEANS FOR SHARING I/O RESOURCES BY A PLURALITY OF OPERATING SYSTEMS
97.	5,410,695	PARALLEL SYSPLEX ARCHITECTURE	APPARATUS AND METHOD FOR LIST MANAGEMENT IN A COUPLED DATA PROCESSING SYSTEM
98.	5,394,554	PARALLEL SYSPLEX ARCHITECTURE	INTERDICTING I/O AND MESSAGING OPERATIONS FROM SENDING CENTRAL PROCESSING COMPLEX TO OTHER CENTRAL PROCESSING COMPLEXES AND TO I/O DEVICE IN MULTI-SYSTEM COMPLEX
99.	5,394,542	PARALLEL SYSPLEX ARCHITECTURE	CLEARING DATA OBJECTS USED TO MAINTAIN STATE INFORMATION FOR SHARED DATA AT A LOCAL COMPLEX WHEN AT LEAST ONE MESSAGE PATH TO THE LOCAL COMPLEX CANNOT BE RECOVERED
100.	5,392,397	PARALLEL SYSPLEX ARCHITECTURE	COMMAND EXECUTION SYSTEM FOR USING FIRST AND SECOND COMMANDS TO RESERVE AND STORE SECOND COMMAND RELATED STATUS INFORMATION IN MEMORY PORTION RESPECTIVELY
101.	5,381,535	VIRTUALIZATION ARCHITECTURE	DATA PROCESSING CONTROL OF SECOND-LEVEL QUEST VIRTUAL MACHINES WITHOUT HOST INTERVENTION
102.	5,361,356	INSTRUCTION SET ARCHITECTURE	STORAGE ISOLATION WITH SUBSPACE-GROUP FACILITY
103.	5,339,405	PARALLEL SYSPLEX ARCHITECTURE	COMMAND QUIESCE FUNCTION
104.	5,331,673	PARALLEL SYSPLEX ARCHITECTURE	INTEGRITY OF DATA OBJECTS USED TO MAINTAIN STATE INFORMATION FOR SHARED DATA AT A LOCAL COMPLEX
105.	5,317,739	PARALLEL SYSPLEX ARCHITECTURE	METHOD AND APPARATUS FOR COUPLING DATA PROCESSING SYSTEMS
106.	5,220,669	OTHER ARCHITECTURE	LINKAGE MECHANISM FOR PROGRAM ISOLATION
107.	App. 12/029514	INSTRUCTION SET ARCHITECTURE	SECURITY MESSAGE AUTHENTICATION INSTRUCTION
108.	App. 12/030912	CHANNEL SUBSYSTEM ARCHITECTURE	DETERMINING EXTENDED CAPABILITY OF A CHANNEL PATH
109.	App. 12/030954	CHANNEL SUBSYSTEM ARCHITECTURE	BI-DIRECTIONAL DATA TRANSFER WITHIN A SINGLE I/O OPERATION
110.	App. 12/031038	CHANNEL SUBSYSTEM ARCHITECTURE	PROVIDING INDIRECT DATA ADDRESSING IN AN INPUT/OUTPUT PROCESSING SYSTEM WHERE THE INDIRECT DATA ADDRESS LIST IS NON-CONTIGUOUS
111.	App. 12/031201	CHANNEL SUBSYSTEM ARCHITECTURE	PROVIDING INDIRECT DATA ADDRESSING FOR A CONTROL BLOCK AT A CHANNEL SUBSYSTEM OF AN I/O PROCESSING SYSTEM
112.	App. 12/036725	VIRTUALIZATION ARCHITECTURE	OPTIMIZATIONS OF A PERFORM FRAME MANAGEMENT FUNCTION ISSUED BY PAGEABLE GUESTS

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
113.	App. 12/037177	VIRTUALIZATION ARCHITECTURE	SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR PROVIDING A SHARED MEMORY TRANSLATION FACILITY
114.	App. 12/037268	VIRTUALIZATION ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH TRANSLATION EXCEPTION QUALIFIER
115.	App. 12/052675	VIRTUALIZATION ARCHITECTURE	MANAGING USE OF STORAGE BY MULTIPLE PAGEABLE GUESTS OF A COMPUTING ENVIRONMENT
116.	App. 12/052683	VIRTUALIZATION ARCHITECTURE	USE OF TEST PROTECTION INSTRUCTION IN COMPUTING ENVIRONMENTS THAT SUPPORT PAGEABLE GUESTS
117.	App. 11/182570	VIRTUALIZATION ARCHITECTURE	FACILITATING PROCESSING WITHIN COMPUTING ENVIRONMENTS SUPPORTING PAGEABLE GUESTS
118.	App. 11/223641	INSTRUCTION SET ARCHITECTURE	FUSED MULTIPLY ADD SPLIT FOR MULTIPLE PRECISION ARITHMETIC
119.	App. 12/363825	INSTRUCTION SET ARCHITECTURE	MULTIFUNCTION HEXADECIMAL INSTRUCTION FORM SYSTEM AND PROGRAM PRODUCT
120.	App. 12/394579	INSTRUCTION SET ARCHITECTURE	CIPHER MESSAGE ASSIST INSTRUCTION
121.	App. 12/417943	INSTRUCTION SET ARCHITECTURE	PARSING-ENHANCEMENT FACILITY
122.	App. 11/437220	INSTRUCTION SET ARCHITECTURE	EXTRACT CPU TIME FACILITY
123.	App. 12/488670	INSTRUCTION SET ARCHITECTURE	STORE CLOCK AND STORE CLOCK FAST INSTRUCTION EXECUTION
124.	App. 11/469573	CHANNEL SUBSYSTEM ARCHITECTURE	GATHERING I/O MEASUREMENT DATA DURING AN I/O OPERATION PROCESS
125.	App. 11/469916	INSTRUCTION SET ARCHITECTURE	METHOD OF EMPLOYING INSTRUCTIONS TO CONVERT UTF CHARACTERS WITH AN ENHANCED EXTENDED TRANSLATION FACILITY
126.	App. 11/469919	INSTRUCTION SET ARCHITECTURE	METHOD OF TRANSLATING N TO N INSTRUCTIONS EMPLOYING AN ENHANCED EXTENDED TRANSLATION FACILITY
127.	App. 12/540261	INSTRUCTION SET ARCHITECTURE	PERFORMING A PERFORM TIMING FACILITY FUNCTION INSTRUCTION FOR SYCHRONIZING TOD CLOCKS
128.	App. 12/555974	INSTRUCTION SET ARCHITECTURE	COMPARE, SWAP AND STORE FACILITY WITH NO EXTERNAL SERIALIZATION
129.	App. 11/532172	INSTRUCTION SET ARCHITECTURE	METHOD AND SYSTEM OF RECORDING TIME OF DAY CLOCK
130.	App. 11/532177	INSTRUCTION SET ARCHITECTURE	ENHANCED STORE FACILITY LIST SYSTEM AND OPERATION
131.	App. 11/551292	INSTRUCTION SET ARCHITECTURE	MESSAGE DIGEST INSTRUCTION
132.	App. 11/680894	INSTRUCTION SET ARCHITECTURE	ROUND FOR REROUND MODE IN A DECIMAL FLOATING POINT INSTRUCTION
133.	App. 11/692382	INSTRUCTION SET ARCHITECTURE	OPTIONAL FUNCTION MULTI-FUNCTION INSTRUCTION
134.	App. 11/733224	MEMORY ARCHITECTURE	CLEARING SELECTED STORAGE TRANSLATION BUFFER ENTRIES BASED ON TABLE ORIGIN ADDRESS
135.	App. 11/740165	INSTRUCTION SET ARCHITECTURE	DETECTION OF POTENTIAL NEED TO USE A LARGER DATA FORMAT IN PERFORMING FLOATING POINT OPERATIONS
136.	App.	INSTRUCTION SET	MANAGEMENT OF EXCEPTIONS AND HARDWARE

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
	11/740185	ARCHITECTURE	INTERRUPTIONS BY AN EXCEPTION SIMULATOR
137.	App. 11/740683	INSTRUCTION SET ARCHITECTURE	INSERT/EXTRACT BIASED EXPONENT OF DECIMAL FLOATING POINT DATA
138.	App. 11/740701	INSTRUCTION SET ARCHITECTURE	SHIFT SIGNIFICAND OF DECIMAL FLOATING POINT DATA
139.	App. 11/740711	INSTRUCTION SET ARCHITECTURE	COMPOSITION/ DECOMPOSITION OF DECIMAL FLOATING POINT DATA
140.	App. 11/740721	INSTRUCTION SET ARCHITECTURE	CONVERT SIGNIFICAND OF DECIMAL FLOATING POINT DATA TO/FROM PACKED DECIMAL FORMAT
141.	App. 11/770861	INSTRUCTION SET ARCHITECTURE	EXTRACT BIASED EXPONENT OF DECIMAL FLOATING POINT DATA
142.	App. 11/781574	INSTRUCTION SET ARCHITECTURE	CONVERT SIGNIFICAND OF DECIMAL FLOATING POINT DATA TO PACKED DECIMAL FORMAT
143.	App. 11/781650	INSTRUCTION SET ARCHITECTURE	CONVERT SIGNIFICAND OF DECIMAL FLOATING POINT DATA FROM PACKED DECIMAL FORMAT
144.	App. 11/840323	INSTRUCTION SET ARCHITECTURE	COMPOSITION OF DECIMAL FLOATING POINT DATA, AND METHODS THEREFORE
145.	App. 11/840345	INSTRUCTION SET ARCHITECTURE	DECOMPOSITION OF DECIMAL FLOATING POINT DATA
146.	App. 11/840359	INSTRUCTION SET ARCHITECTURE	DECOMPOSITION OF DECIMAL FLOATING POINT DATA, AND METHODS THEREFORE
147.	App. 11/868605	INSTRUCTION SET ARCHITECTURE	PERFORM FLOATING POINT OPERATION INSTRUCTION
148.	App. 10/854990	VIRTUALIZATION ARCHITECTURE	FACILITATING MANAGEMENT OF STORAGE OF A PAGEABLE MODE VIRTUAL ENVIRONMENT ABSENT INTERVENTION OF A HOST OF THE ENVIRONMENT
149.	App. 10/855200	VIRTUALIZATION ARCHITECTURE	INTERPRETING I/O OPERATION REQUESTS FROM PAGEABLE GUESTS WITHOUT HOST INTERVENTION
150.	App. 11/954526	INSTRUCTION SET ARCHITECTURE	PRE-FETCH DATA AND PRE-FETCH DATA RELATIVE
151.	App. 11/965866	CHANNEL SUBSYSTEM ARCHITECTURE	EXTENDED INPUT/OUTPUT MEASUREMENT WORD FACILITY, AND EMULATION OF THAT FACILITY
152.	App. 11/968733	INSTRUCTION SET ARCHITECTURE	SYSTEM AND METHOD FOR TOD-CLOCK STEERING
153.	App. 11/972666	INSTRUCTION SET ARCHITECTURE	COMPARE AND BRANCH FACILITY AND INSTRUCTION THEREFORE
154.	App. 11/972675	INSTRUCTION SET ARCHITECTURE	EXTRACT CACHE ATTRIBUTE FACILITY AND INSTRUCTION THEREFORE
155.	App. 11/972679	INSTRUCTION SET ARCHITECTURE	ROTATE THEN OPERATE ON SELECTED BITS FACILITY AND INSTRUCTIONS THEREFORE
156.	App. 11/972682	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH ACCESS CONTROL
157.	App. 11/972688	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH FETCH PROTECTION
158.	App. 11/972689	INSTRUCTION SET ARCHITECTURE	ROTATE THEN INSERT SELECTED BITS FACILITY AND INSTRUCTIONS THEREFORE
159.	App. 11/972694	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH CHANGE RECORDING OVERRIDE
160.	App. 11/972697	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH FORMAT CONTROL
161.	App.	MEMORY	DYNAMIC ADDRESS TRANSLATION WITH LOAD

NO.	US PATENT OR APPLICATION NO.	FEATURE TYPE	TITLE
	11/972700	ARCHITECTURE	PAGE TABLE ENTRY ADDRESS
162.	App. 11/972705	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH LOAD REAL ADDRESS
163.	App. 11/972706	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH FORMAT CONTROL
164.	App. 11/972713	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH FRAME MANAGEMENT
165.	App. 11/972714	INSTRUCTION SET ARCHITECTURE	EXECUTE RELATIVE LONG FACILITY AND INSTRUCTIONS THEREFORE
166.	App. 11/972715	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH DAT PROTECTION
167.	App. 11/972718	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH FRAME MANAGEMENT
168.	App. 11/972725	MEMORY ARCHITECTURE	DYNAMIC ADDRESS TRANSLATION WITH FRAME MANAGEMENT
169.	App. 11/972740	INSTRUCTION SET ARCHITECTURE	LOAD RELATIVE AND STORE RELATIVE FACILITY AND INSTRUCTIONS THEREFORE
170.	App. 11/972766	INSTRUCTION SET ARCHITECTURE	PERFORMING A CONFIGURATION VIRTUAL TOPOLOGY CHANGE AND INSTRUCTION THEREFORE
171.	App. 11/972780	INSTRUCTION SET ARCHITECTURE	COMPARE RELATIVE LONG FACILITY AND INSTRUCTIONS THEREFORE
172.	App. 11/972791	INSTRUCTION SET ARCHITECTURE	MOVE FACILITY AND INSTRUCTIONS THEREFORE
173.	App. 11/972802	INSTRUCTION SET ARCHITECTURE	COMPUTER CONFIGURATION VIRTUAL TOPOLOGY DISCOVERY AND INSTRUCTION THEREFORE