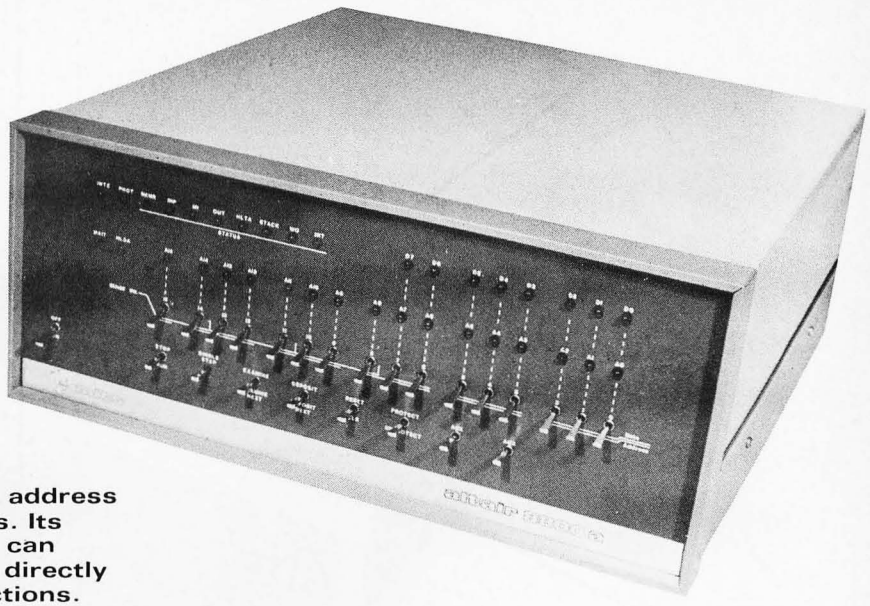
altair T.M. 8800a

TECHNICAL INFORMATION



The Altair 8800a is a parallel 8-bit word/16-bit address computer with an instruction cycle time of 2 μs. Its central processing unit is the 8080 LSI chip. It can accommodate 256 inputs and 256 outputs, all directly addressable, and has 78 basic machine instructions. It is capable of directly addressing up to 65,000 bytes of memory.

As well as the LSI chip, the CPU board contains the two-phase clock, status latch, buffers and the various lines going to the bus. (The buffers are tri-state devices.)

The CPU contains six general-purpose registers, P counter, arithmetic unit, accumulator, stack pointer, instruction decoder, and miscellaneous timing and control circuits. The arithmetic unit contains the circuitry required to perform arithmetic in both decimal and binary forms. The stack pointer defines the current address of the external stack, which resides in memory. The stack is used to service interrupts and provides virtually unlimited subroutine nesting. The instruction decoder decodes the instructions and sets up the various registers, gates, etc., in the CPU for proper functioning.

There are 36 LED status indicators on the front panel, 16 of which are used for the address bus, 8 for the system status latches, and 8 for the data bus. The four remaining LEDs are used for indicating memory-protect, interrupt-enable, system-wait and hold status. Address line inputs A0 through A15, data lines D0 through D7, and the various status lines originate on the CPU board.

The front panel control board contains the circuitry for interfacing between the control switches located on the front panel and the CPU. In addition to the interconnections to the actual processor, this board accepts memory address switches A0 through A15 (also on the front panel). The first eight of these switches (D0 to D7) are used to put data into the CPU.

The front panel logic permits the following functions: STOP—stops the processor immediately after it completes the current instruction; RUN—starts the processor at the current address; EXAMINE—causes the data stored at the location (set by the switches) to be displayed in binary by LEDs; EXAMINE NEXT—steps the P counter once and displays the word stored at the next location; DEPOSIT—causes the information preset by the switches (A0-A7) to be stored in memory; DEPOSIT NEXT—steps the P counter and loads the memory; SINGLE STEP—steps the program one machine cycle; RESET—clears the CPU and sets up a starting address of 0; PROTECT/UNPROTECT—allows selective write protection of blocks of memory. When a block of memory is protected, it is impossible to write over that block, but its contents can be read out.

With proper adjustments, any memory speed can be used in the 8800a computer, although memory access time must be 500 nanoseconds or less if it is to be run without wait states. In addition to semiconductor RAMs, the processor will also service ROMs and PROMs.

NEW FEATURES

POWER SUPPLY

The power supply provides three voltages to the 8800a bus: +8V pre-regulated at 8 amps; +15V at 500mA; −15V at 500mA.

FAN

A fan has been mounted on the back panel of the 8800a to provide cooler operating temperatures.

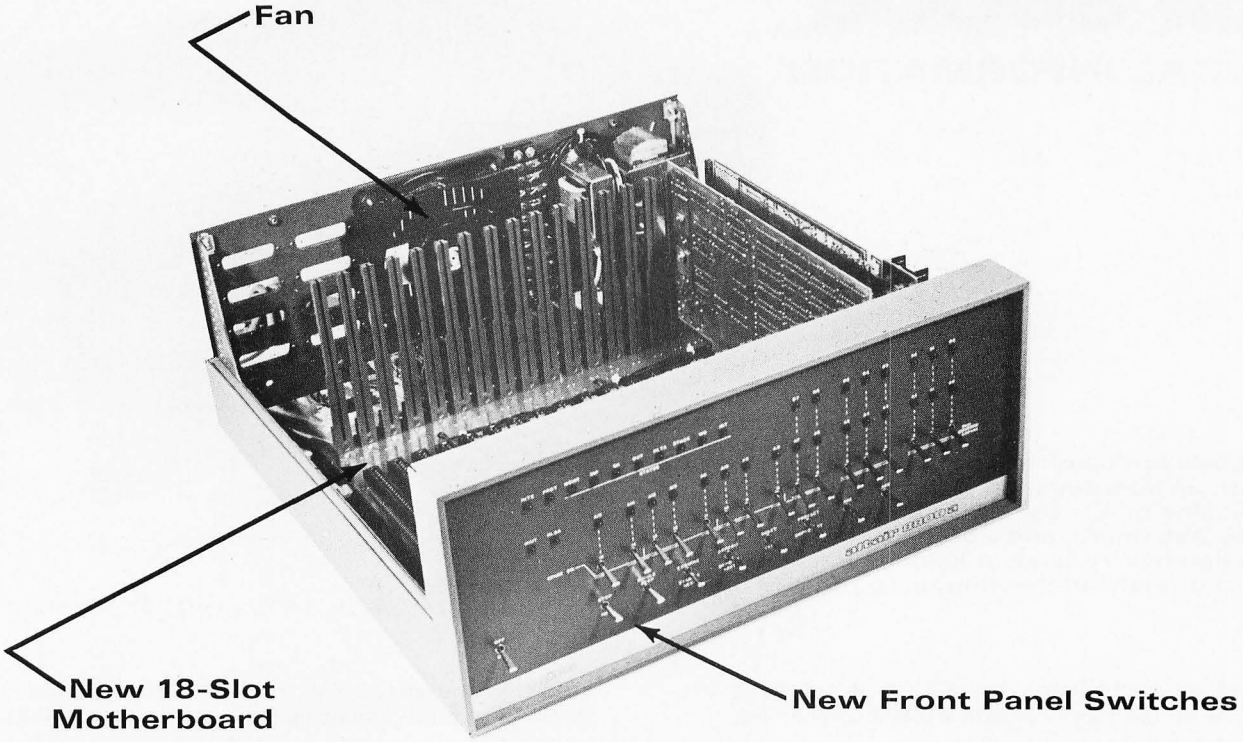
18 SLOT MOTHERBOARD

The four-slot expander cards in the Altair 8800 have been replaced with a single-piece 18-slot motherboard. The 18-slot motherboard contains the 100 solder lands that comprise the 100 pin bus.

FRONT PANEL SWITCHES

The front panel toggle switches have 50% longer handles that are flat (instead of round) for easier use.

An assembled Altair 8800a may be ordered with six, twelve, or eighteen sets of edge connectors. The Altair 8800a kits include an edge connector with every plug-in module purchased.



The four boards, along with the power supply, mount in an 18" deep x 17" wide x 7" high (45.7 x 43.2 x 17.7-cm) metal cabinet.

SPECIFICATIONS

Number of Boards	Up to 18
Microprocessor	
Model	8080A
Technology	NMOS
Data Word Size, Bits	8
Instruction Word Size, Bits	8
Clock Frequency,	2MHz
Add Time, Register to Register, Microsec. Per Data Word	2
Number of Instructions	78
Input/Output Control	
I/O Word Size, Bits	8
Number of I/O Channels	256
Direct Memory Access	Optional
Interrupt Capability	Std. one level
Vectored Interrupt (8 priority levels)	Optional
Software	
Resident Assembler	Yes
Cross Assembler	No
Simulator	No
Higher-level Language	BASIC
Monitor or Executive	Sys. mon.; text edit.
Software Separately Priced	Yes

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